32-Channel, 16-/14-Bit, Serial Input, Voltage Output DAC

AD5372/AD5373

FEATURES

- 32-channel DAC in a 64-lead LQFP and 64-lead LFCSP
- AD5372/AD5373[1] guaranteed monotonic to 16/14 bits
- Maximum output voltage span of 4 × VREF (20 V)
- Nominal output voltage range of −4 V to +8 V
- Multiple, independent output voltage spans available
- System calibration function allowing user-programmable offset and gain
- Channel grouping and addressing features
- Thermal shutdown function
- DSP/microcontroller-compatible serial interface
- SPI serial interface
- 2.5 V to 5.5 V JEDEC-compliant digital levels
- Digital reset ($\overline{\text{RESET}}$)
- Clear function to user-defined SIGGNDx
- Simultaneous update of DAC outputs

APPLICATIONS

- Level setting in automatic test equipment (ATE)
- Variable optical attenuators (VOA)
- Optical switches
- Industrial control systems
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM

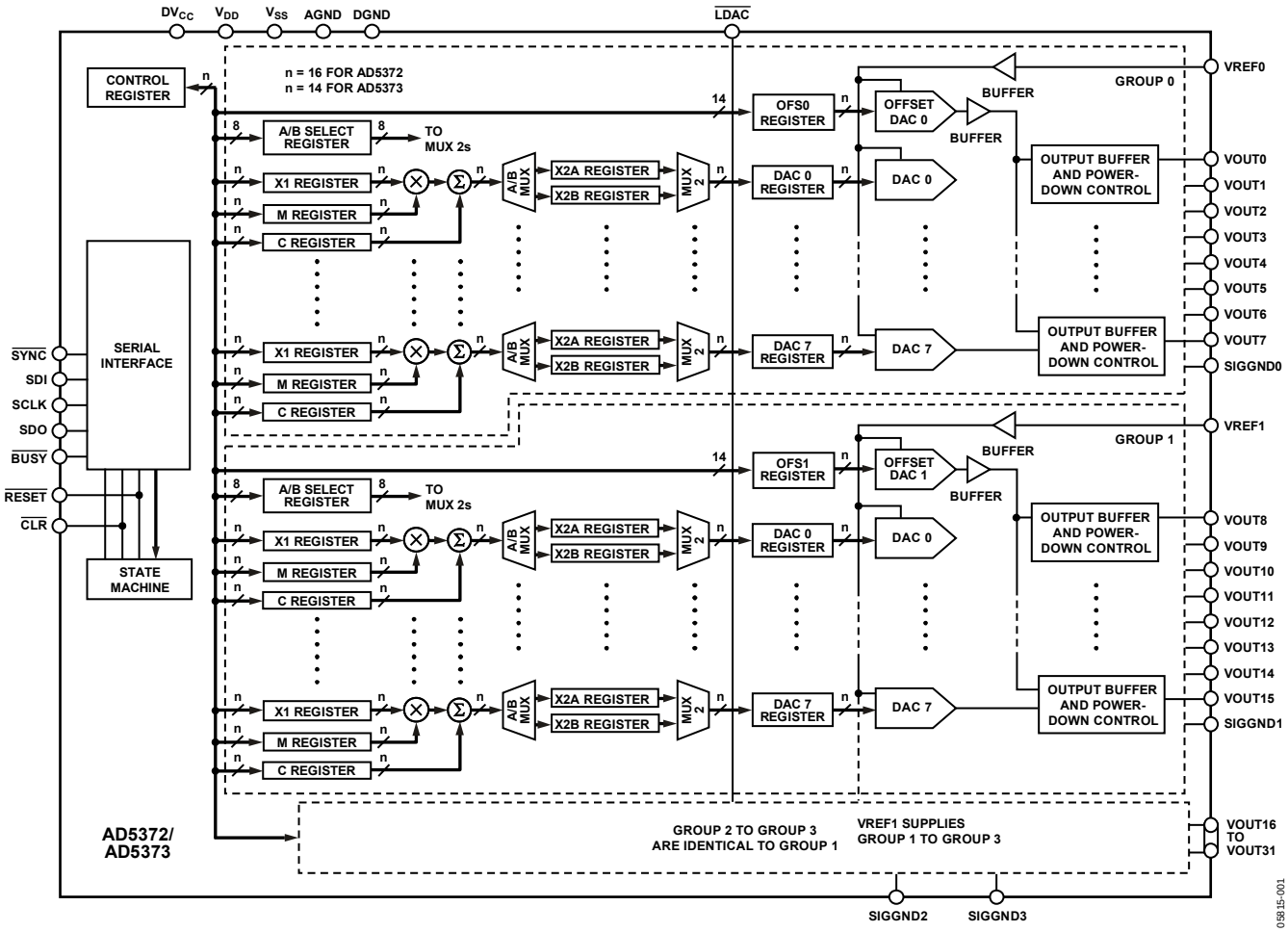

Figure 1.

[1] Protected by U.S. Patent No. 5,969,657.

Rev. C

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
Functional Block Diagram ... 1
Revision History ... 2
General Description ... 3
Specifications ... 4
AC Characteristics ... 5
Timing Characteristics ... 6
Absolute Maximum Ratings ... 9
ESD Caution ... 9
Pin Configurations and Function Descriptions ... 10
Typical Performance Characteristics ... 12
Terminology ... 14
Theory of Operation ... 15
DAC Architecture ... 15
Channel Groups ... 15
A/B Registers and Gain/Offset Adjustment ... 16
Load DAC ... 16
Offset DACs ... 16
Output Amplifier ... 17
Transfer Function ... 17
Reference Selection ... 17
Calibration ... 18
Additional Calibration ... 19
Reset Function ... 19
Clear Function ... 19
$\overline{\text{BUSY}}$ and $\overline{\text{LDAC}}$ Functions ... 19
Power-Down Mode ... 20
Thermal Shutdown Function ... 20
Toggle Mode ... 20
Serial Interface ... 21
SPI Write Mode ... 21
SPI Readback Mode ... 21
Register Update Rates ... 21
Channel Addressing and Special Modes ... 22
Special Function Mode ... 23
Applications Information ... 24
Power Supply Decoupling ... 24
Power Supply Sequencing ... 24
Interfacing Examples ... 24
Outline Dimensions ... 25
Ordering Guide ... 26

REVISION HISTORY

7/11—Rev. B to Rev. C

Added 64-Lead LFCSP Package ... Universal
Change to Features Section ... 1
Change to General Description Section ... 3
Changes to Table 5 ... 9
Added Figure 7; Renumbered Sequentially ... 10
Changes to Table 6 ... 10
Updated Outline Dimensions ... 24
Changes to Ordering Guide ... 25

2/08—Rev. A to Rev. B

Added Table 1 ... 3
Changes to t_{10} Parameter ... 6
Added t_{23} Parameter ... 6
Changes to Figure 4 ... 7
Changes to Absolute Maximum Ratings Section ... 9
Changes to Pin Configuration and Function Descriptions Section ... 10
Changes to Reset Function Section ... 18

12/07—Rev. 0 to Rev. A

Changes to Table 3 ... 6
Changes to AD5373 Transfer Function Section ... 16
Changes to Calibration Section ... 17
Changes to Table 8 ... 18
Changes to Register Update Rates Section ... 20
Changes to Ordering Guide ... 25

8/07—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD5372/AD5373 contain 32 16-/14-bit DACs in 64-lead LQFP and LFCSP packages. The devices provide buffered voltage outputs with a nominal span of 4× the reference voltage. The gain and offset of each DAC can be independently trimmed to remove errors. For even greater flexibility, the device is divided into four groups of eight DACs. Two offset DACs allow the output range of the groups to be altered. Group 0 can be adjusted by Offset DAC 0, and Group 1 to Group 3 can be adjusted by Offset DAC 1.

The AD5372/AD5373 offer guaranteed operation over a wide supply range: V_{SS} from −16.5 V to −4.5 V and V_{DD} from 9 V to 16.5 V. The output amplifier headroom requirement is 1.4 V operating with a load current of 1 mA.

The AD5372/AD5373 have a high speed serial interface that is compatible with SPI, QSPI™, MICROWIRE™, and DSP interface standards and can handle clock speeds of up to 50 MHz.

The DAC registers are updated on reception of new data. All the outputs can be updated simultaneously by taking the $\overline{\text{LDAC}}$ input low. Each channel has a programmable gain and an offset adjust register.

Each DAC output is gained and buffered on chip with respect to an external SIGGNDx input. The DAC outputs can also be switched to SIGGNDx via the $\overline{\text{CLR}}$ pin.

Table 1. High Channel Count Bipolar DACs

Model	Resolution (Bits)	Nominal Output Span	Output Channels	Linearity Error (LSB)
AD5360	16	$4 \times V_{REF}$ (20 V)	16	±4
AD5361	14	$4 \times V_{REF}$ (20 V)	16	±1
AD5362	16	$4 \times V_{REF}$ (20 V)	8	±4
AD5363	14	$4 \times V_{REF}$ (20 V)	8	±1
AD5370	16	$4 \times V_{REF}$ (12 V)	40	±4
AD5371	14	$4 \times V_{REF}$ (12 V)	40	±1
AD5372	16	$4 \times V_{REF}$ (12 V)	32	±4
AD5373	14	$4 \times V_{REF}$ (12 V)	32	±1
AD5378	14	±8.75 V	32	±3
AD5379	14	±8.75 V	40	±3

SPECIFICATIONS

DV_{CC} = 2.5 V to 5.5 V; V_{DD} = 9 V to 16.5 V; V_{SS} = −16.5 V to −8 V; VREF0 = VREF1 = 3 V; AGND = DGND = SIGGNDx = 0 V; C_L = open circuit; R_L = open circuit; gain (M), offset (C), and DAC offset registers at default values; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	AD5372[1] B Version	AD5373[1] B Version	Unit	Test Conditions/Comments[2]
ACCURACY				
Resolution	16	14	Bits	
Integral Nonlinearity (INL)	±4	±1	LSB max	
Differential Nonlinearity (DNL)	±1	±1	LSB max	Guaranteed monotonic by design over temperature
Zero-Scale Error	±10	±10	mV max	Before calibration
Full-Scale Error	±10	±10	mV max	Before calibration
Gain Error	0.1	0.1	% FSR	Before calibration
Zero-Scale Error[2]	1	1	LSB typ	After calibration
Full-Scale Error[2]	1	1	LSB typ	After calibration
Span Error of Offset DAC	±35	±35	mV max	See the Offset DACS section for details
VOUTx Temperature Coefficient	5	5	ppm FSR/°C typ	Includes linearity, offset, and gain drift
DC Crosstalk[2]	100	100	µV max	Typically 20 µV; measured channel at midscale, full-scale change on any other channel
REFERENCE INPUTS (VREF0, VREF1)[2]				
VREFx Input Current	±10	±10	µA max	Per input; typically ±30 nA
VREFx Range	2/5	2/5	V min/V max	±2% for specified operation
SIGGND INPUTS (SIGGND0 TO SIGGND3)[2]				
DC Input Impedance	50	50	kΩ min	Typically 55 kΩ
Input Range	±0.5	±0.5	V min/V max	
SIGGNDx Gain	0.995/1.005	0.995/1.005	min/max	
OUTPUT CHARACTERISTICS[2]				
Output Voltage Range	V_{SS} + 1.4	V_{SS} + 1.4	V min	I_{LOAD} = 1 mA
	V_{DD} − 1.4	V_{DD} − 1.4	V max	I_{LOAD} = 1 mA
Nominal Output Voltage Range	−4 to +8	−4 to +8	V min/V max	
Short-Circuit Current	15	15	mA max	VOUTx to DV_{CC}, V_{DD}, or V_{SS}
Load Current	±1	±1	mA max	
Capacitive Load	2200	2200	pF max	
DC Output Impedance	0.5	0.5	Ω max	
DIGITAL INPUTS				JEDEC compliant
Input High Voltage	1.7	1.7	V min	DV_{CC} = 2.5 V to 3.6 V
	2.0	2.0	V min	DV_{CC} = 3.6 V to 5.5 V
Input Low Voltage	0.8	0.8	V max	DV_{CC} = 2.5 V to 5.5 V
Input Current	±1	±1	µA max	Excluding $\overline{CLR}$ pin
$\overline{CLR}$ High Impedance Leakage Current	±20	±20	µA max	
Input Capacitance[2]	10	10	pF max	
DIGITAL OUTPUTS (SDO, $\overline{BUSY}$)				
Output Low Voltage	0.5	0.5	V max	Sinking 200 µA
Output High Voltage (SDO)	DV_{CC} − 0.5	DV_{CC} − 0.5	V min	Sourcing 200 µA
SDO High Impedance Leakage Current	±5	±5	µA max	
High Impedance Output Capacitance[2]	10	10	pF typ	

Parameter	AD5372[1] B Version	AD5373[1] B Version	Unit	Test Conditions/Comments[2]
POWER REQUIREMENTS				
DV_{CC}	2.5/5.5	2.5/5.5	V min/V max	
V_{DD}	9/16.5	9/16.5	V min/V max	
V_{SS}	−16.5/−4.5	−16.5/−4.5	V min/V max	
Power Supply Sensitivity[2]				
ΔFull Scale/ΔV_{DD}	−75	−75	dB typ	
ΔFull Scale/ΔV_{SS}	−75	−75	dB typ	
ΔFull Scale/ΔDV_{CC}	−90	−90	dB typ	
DI_{CC}	2	2	mA max	DV_{CC} = 5.5 V, $V_{IH} = DV_{CC}$, V_{IL} = GND
I_{DD}	16	16	mA max	Outputs unloaded, DAC outputs = 0 V
	18	18	mA max	Outputs unloaded, DAC outputs = full scale
I_{SS}	−16	−16	mA max	Outputs unloaded, DAC outputs = 0 V
	−18	−18	mA max	Outputs unloaded, DAC outputs = full scale
Power-Down Mode				Bit 0 in the control register is 1
DI_{CC}	5	5	µA typ	
I_{DD}	35	35	µA typ	
I_{SS}	−35	−35	µA typ	
Power Dissipation (Unloaded)	250	250	mW typ	V_{SS} = −8 V, V_{DD} = 9.5 V, DV_{CC} = 2.5 V
Junction Temperature[3]	130	130	°C max	$T_J = T_A + P_{TOTAL} \times \theta_{JA}$

[1] Temperature range for B version: −40°C to +85°C. Typical specifications are at 25°C.
[2] Guaranteed by design and characterization; not production tested.
[3] θ_{JA} represents the package thermal impedance.

AC CHARACTERISTICS

DV_{CC} = 2.5 V; V_{DD} = 15 V; V_{SS} = −15 V; VREF0 = VREF1 = 3 V; AGND = DGND = SIGGNDx = 0 V; C_L = 200 pF; R_L = 10 kΩ; gain (M), offset (C), and DAC offset registers at default values; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	B Version	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[1]			
Output Voltage Settling Time	20	µs typ	Full-scale change
	30	µs max	DAC latch contents alternately loaded with all 0s and all 1s
Slew Rate	1	V/µs typ	
Digital-to-Analog Glitch Energy	5	nV-s typ	
Glitch Impulse Peak Amplitude	10	mV max	
Channel-to-Channel Isolation	100	dB typ	VREF0, VREF1 = 2 V p-p, 1 kHz
DAC-to-DAC Crosstalk	10	nV-s typ	
Digital Crosstalk	0.2	nV-s typ	
Digital Feedthrough	0.02	nV-s typ	Effect of input bus activity on DAC output under test
Output Noise Spectral Density @ 10 kHz	250	nV/√Hz typ	VREF0 = VREF1 = 0 V

[1] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

DV_{CC} = 2.5 V to 5.5 V; V_{DD} = 9 V to 16.5 V; V_{SS} = −16.5 V to −8 V; VREFx = 3 V; AGND = DGND = SIGGNDx = 0 V; C_L = 200 pF to GND; R_L = open circuit; gain (M), offset (C), and DAC offset registers at default values; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4. SPI Interface

Parameter [1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	20	ns min	SCLK cycle time
t_2	8	ns min	SCLK high time
t_3	8	ns min	SCLK low time
t_4	11	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	20	ns min	Minimum $\overline{SYNC}$ high time
t_6	10	ns min	24th SCLK falling edge to $\overline{SYNC}$ rising edge
t_7	5	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9 [4]	42	ns max	$\overline{SYNC}$ rising edge to $\overline{BUSY}$ falling edge
t_{10}	1/1.5	µs typ/µs max	$\overline{BUSY}$ pulse width low (single-channel update); see Table 9
t_{11}	600	ns max	Single-channel update cycle time
t_{12}	20	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
t_{13}	10	ns min	$\overline{LDAC}$ pulse width low
t_{14}	3	µs max	$\overline{BUSY}$ rising edge to DAC output response time
t_{15}	0	ns min	$\overline{BUSY}$ rising edge to $\overline{LDAC}$ falling edge
t_{16}	3	µs max	$\overline{LDAC}$ falling edge to DAC output response time
t_{17}	20/30	µs typ/µs max	DAC output settling time
t_{18}	140	ns max	$\overline{CLR}$/$\overline{RESET}$ pulse activation time
t_{19}	30	ns min	$\overline{RESET}$ pulse width low
t_{20}	400	µs max	$\overline{RESET}$ time indicated by $\overline{BUSY}$ low
t_{21}	270	ns min	Minimum $\overline{SYNC}$ high time in readback mode
t_{22} [5]	25	ns max	SCLK rising edge to SDO valid
t_{23}	80	ns max	$\overline{RESET}$ rising edge to $\overline{BUSY}$ falling edge

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 4 and Figure 5.
[4] t_9 is measured with the load circuit shown in Figure 2.
[5] t_{22} is measured with the load circuit shown in Figure 3.

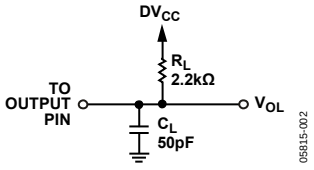


Figure 2. Load Circuit for $\overline{BUSY}$ Timing Diagram

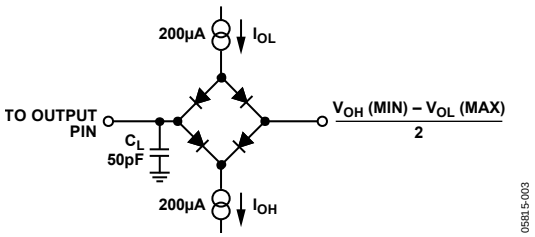


Figure 3. Load Circuit for SDO Timing Diagram

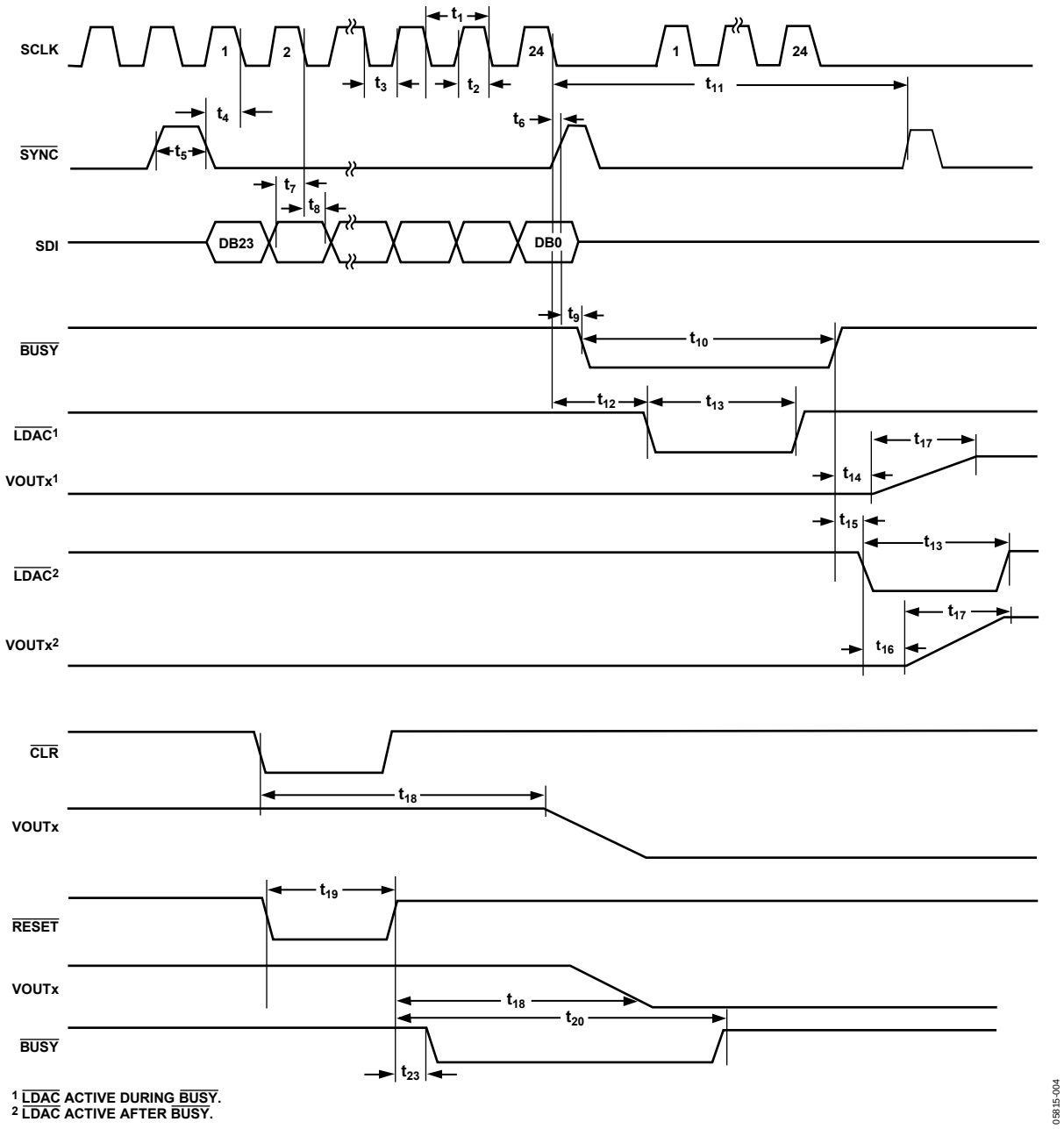


Figure 4. SPI Write Timing

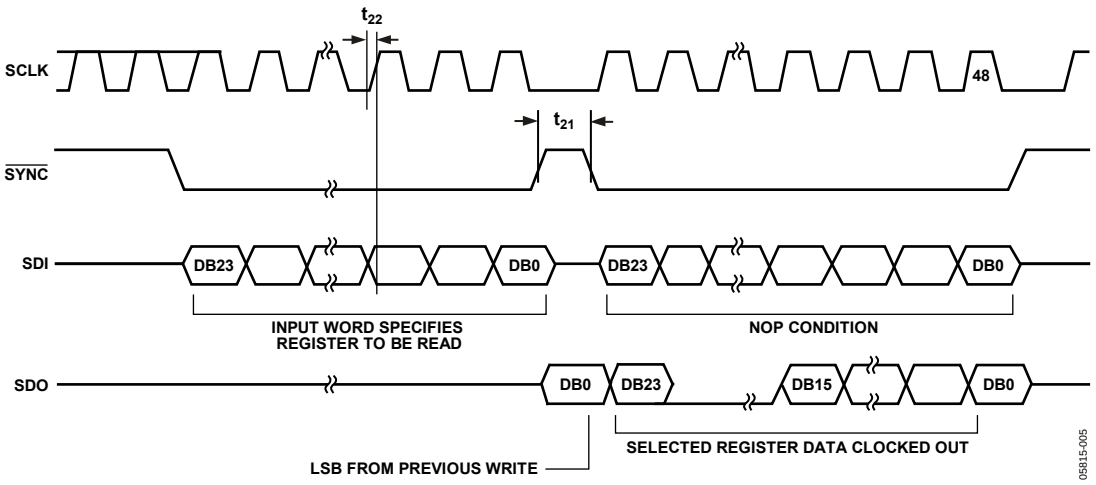


Figure 5. SPI Read Timing

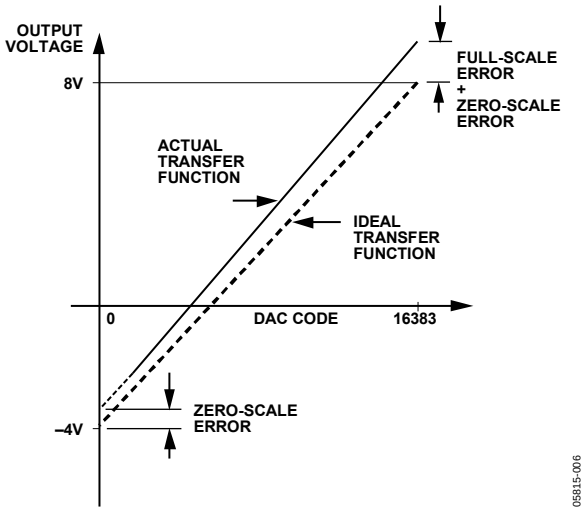


Figure 6. DAC Transfer Function

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 60 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +17 V
V_{SS} to AGND	−17 V to +0.3 V
DV_{CC} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DV_{CC} + 0.3 V
Digital Outputs to DGND	−0.3 V to DV_{CC} + 0.3 V
VREF0, VREF1 to AGND	−0.3 V to +5.5 V
VOUT0 through VOUT31 to AGND	V_{SS} − 0.3 V to V_{DD} + 0.3 V
SIGGNDx to AGND	−1 V to +1 V
AGND to DGND	−0.3 V to +0.3 V
Operating Temperature Range (T_A)	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	130°C
θ_{JA} Thermal Impedance	
64-Lead LFCSP	25.5°C/W
64-Lead LQFP	45.5°C/W
Reflow Soldering	
Peak Temperature	230°C
Time at Peak Temperature	10 sec to 40 sec

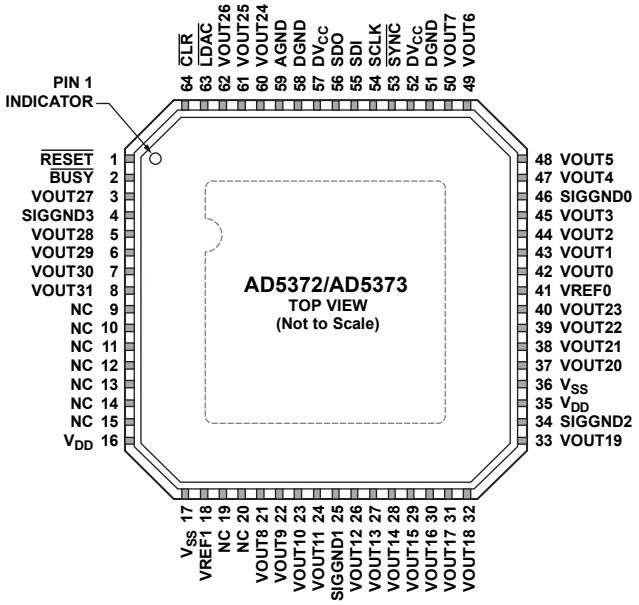
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. THE LEAD FRAME CHIP SCALE PACKAGE (LFCSP) HAS AN EXPOSED PAD ON THE UNDERSIDE. CONNECT THE EXPOSED PAD TO V_{SS}.

Figure 7. 64-Lead LFCSP Pin Configuration

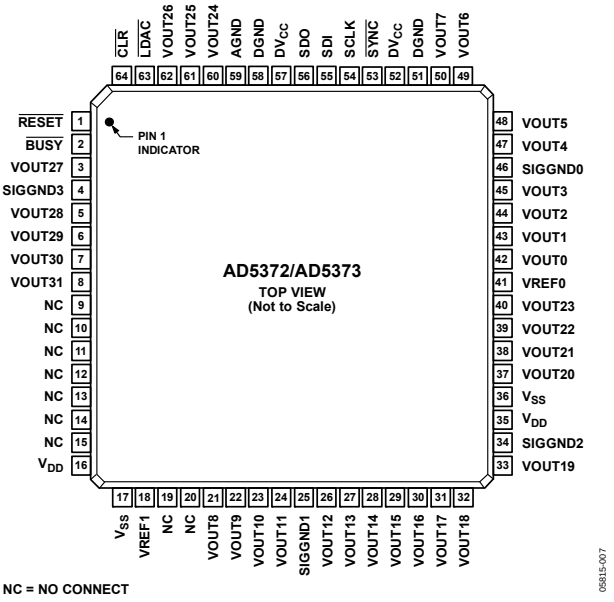


Figure 8. 64-Lead LQFP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	EPAD	Exposed Pad. The lead frame chip scale package (LFCSP) has an exposed pad on the underside. Connected the exposed pad to V_{SS}.
1	$\overline{\text{RESET}}$	Digital Reset Input.
2	$\overline{\text{BUSY}}$	Digital Input/Open-Drain Output. $\overline{\text{BUSY}}$ is open drain when an output. See the $\overline{\text{BUSY}}$ and $\overline{\text{LDAC}}$ Functions section for more information.
42 to 45, 47 to 50, 21 to 24, 26 to 33, 37 to 40, 60 to 62, 3, 5 to 8	VOUT0 to VOUT31	DAC Outputs. Buffered analog outputs for each of the 32 DAC channels. Each analog output is capable of driving an output load of 10 kΩ to ground. Typical output impedance of these amplifiers is 0.5 Ω.
4	SIGGND3	Reference Ground for DAC 24 to DAC 31. VOUT24 to VOUT31 are referenced to this voltage.
9 to 15, 19, 20	NC	No Connect.
16, 35	V_{DD}	Positive Analog Power Supply; 9 V to 16.5 V for specified performance. These pins should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
17, 36	V_{SS}	Negative Analog Power Supply; −16.5 V to −8 V for specified performance. These pins should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
18	VREF1	Reference Input for DAC 8 to DAC 31. This reference voltage is referred to AGND.
25	SIGGND1	Reference Ground for DAC 8 to DAC 15. VOUT8 to VOUT15 are referenced to this voltage.
34	SIGGND2	Reference Ground for DAC 16 to DAC 23. VOUT16 to VOUT23 are referenced to this voltage.
41	VREF0	Reference Input for DAC 0 to DAC 7. This reference voltage is referred to AGND.
46	SIGGND0	Reference Ground for DAC 0 to DAC 7. VOUT0 to VOUT7 are referenced to this voltage.
51, 58	DGND	Ground for All Digital Circuitry. The DGND pins should be connected to the DGND plane.
52, 57	DV_{CC}	Logic Power Supply; 2.5 V to 5.5 V. These pins should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
53	$\overline{\text{SYNC}}$	Active Low Input. This is the frame synchronization signal for the serial interface.
54	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of SCLK. This pin operates at clock speeds up to 50 MHz.
55	SDI	Serial Data Input. Data must be valid on the falling edge of SCLK.

Pin No.	Mnemonic	Description
56	SDO	Serial Data Output. CMOS output. SDO can be used for readback. Data is clocked out on SDO on the rising edge of SCLK and is valid on the falling edge of SCLK.
59	AGND	Ground for All Analog Circuitry. The AGND pin should be connected to the AGND plane.
63	$\overline{\text{LDAC}}$	Load DAC Logic Input (Active Low). See the $\overline{\text{BUSY}}$ and $\overline{\text{LDAC}}$ Functions section for more information.
64	$\overline{\text{CLR}}$	Asynchronous Clear Input (Level Sensitive, Active Low). See the Clear Function section for more information.

TYPICAL PERFORMANCE CHARACTERISTICS

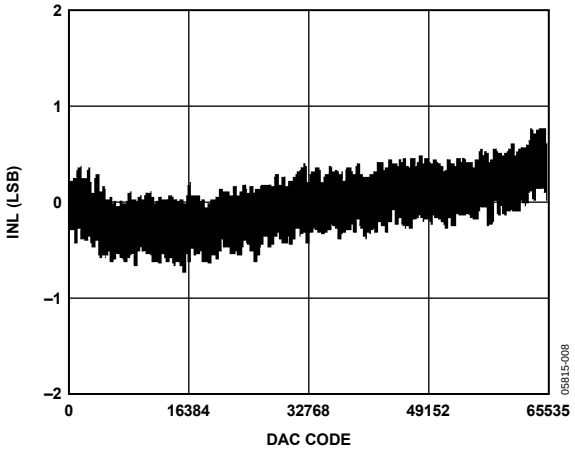


Figure 9. Typical AD5372 INL Plot

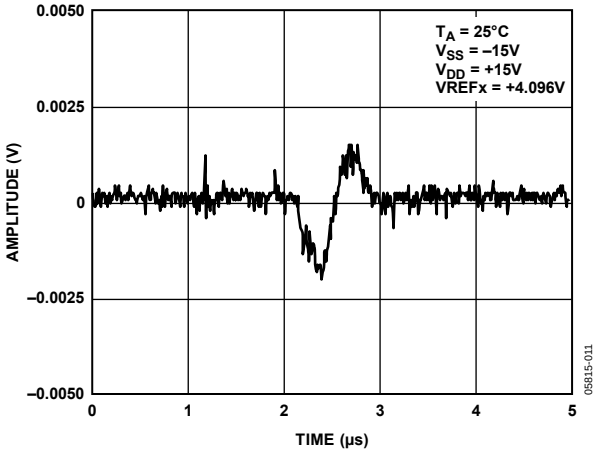


Figure 12. Digital Crosstalk

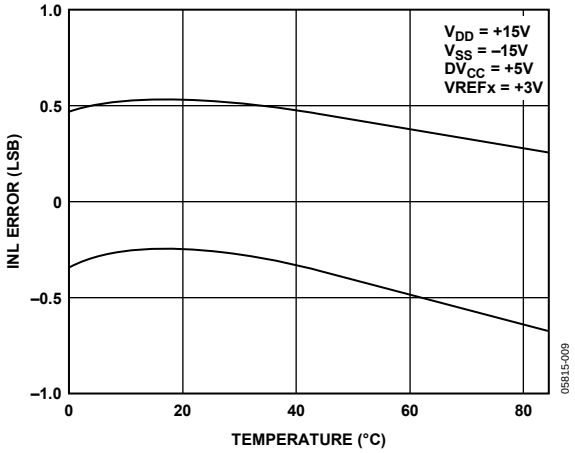


Figure 10. Typical INL Error vs. Temperature

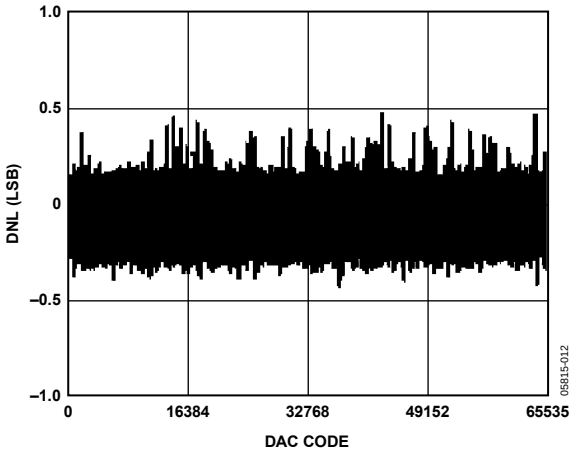


Figure 13. Typical AD5372 DNL Plot

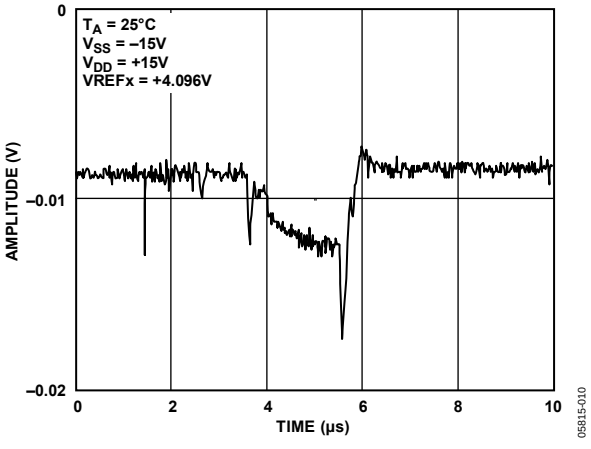


Figure 11. Analog Crosstalk Due to $\overline{LDAC}$

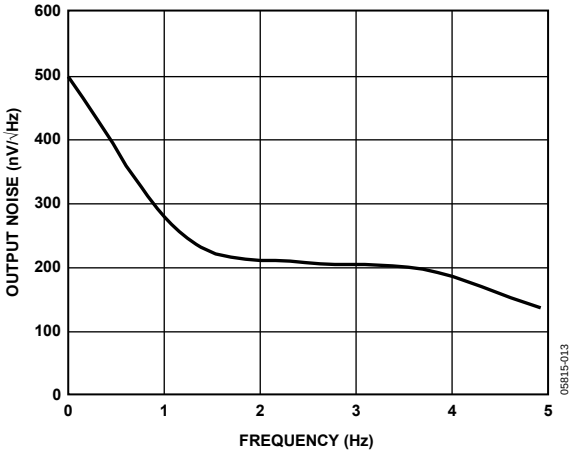


Figure 14. Output Noise Spectral Density

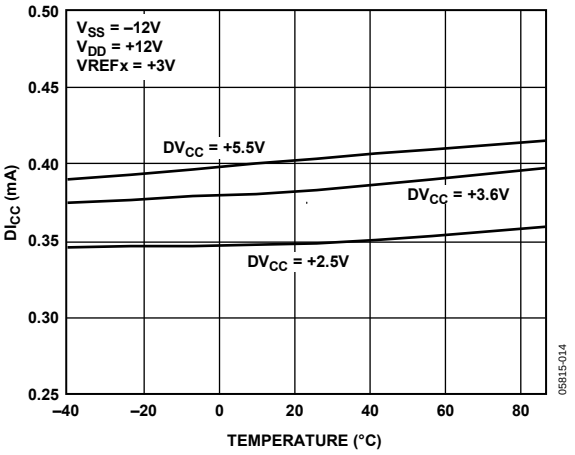


Figure 15. DI_{CC} vs. Temperature

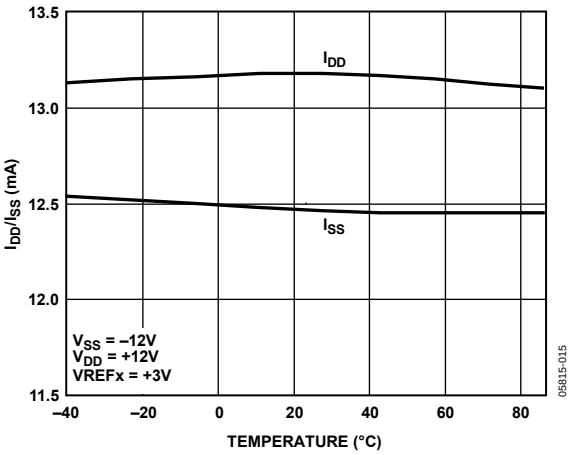


Figure 16. I_{DD}/I_{SS} vs. Temperature

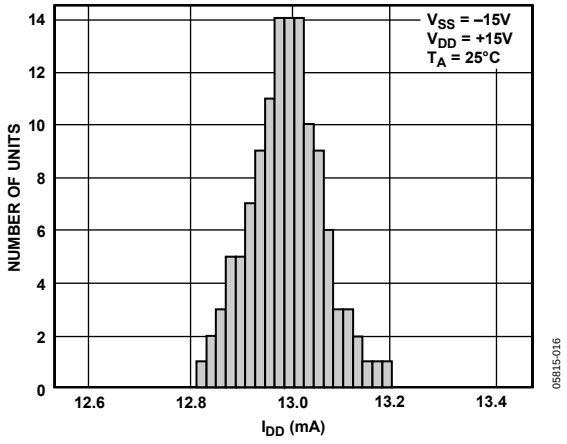


Figure 17. Typical I_{DD} Distribution

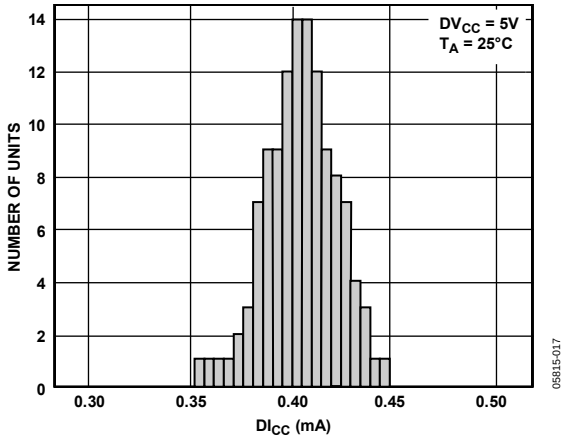


Figure 18. Typical DI_{CC} Distribution

TERMINOLOGY

Integral Nonlinearity (INL)
Integral nonlinearity, or endpoint linearity, is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error and is expressed in least significant bits (LSB).

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Zero-Scale Error
Zero-scale error is the error in the DAC output voltage when all 0s are loaded into the DAC register. Zero-scale error is a measure of the difference between VOUT (actual) and VOUT (ideal), expressed in millivolts, when the channel is at its minimum value. Zero-scale error is mainly due to offsets in the output amplifier.

Full-Scale Error
Full-scale error is the error in the DAC output voltage when all 1s are loaded into the DAC register. Full-scale error is a measure of the difference between VOUT (actual) and VOUT (ideal), expressed in millivolts, when the channel is at its maximum value. Full-scale error does not include zero-scale error.

Gain Error
Gain error is the difference between full-scale error and zero-scale error. It is expressed as a percentage of the full-scale range (FSR).

Gain Error = Full-Scale Error – Zero-Scale Error

VOUT Temperature Coefficient
The VOUT temperature coefficient includes output error contributions from linearity, offset, and gain drift.

DC Output Impedance
DC output impedance is the effective output source resistance. It is dominated by package lead resistance.

DC Crosstalk
The DAC outputs are buffered by op amps that share common V_{DD} and V_{SS} power supplies. If the dc load current changes in one channel (due to an update), this change can result in a further dc change in one or more channel outputs. This effect is more significant at high load currents and is reduced as the load currents are reduced. With high impedance loads, the effect is virtually immeasurable. Multiple V_{DD} and V_{SS} terminals are provided to minimize dc crosstalk.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Energy
Digital-to-analog glitch energy is the amount of energy that is injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 0x7FFF and 0x8000 (AD5372) or 0x1FFF and 0x2000 (AD5373).

Channel-to-Channel Isolation
Channel-to-channel isolation refers to the proportion of input signal from the reference input of one DAC that appears at the output of another DAC operating from another reference. It is expressed in decibels and measured at midscale.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse that appears at the output of one converter due to both the digital change and subsequent analog output change at another converter. It is specified in nV-s.

Digital Crosstalk
Digital crosstalk is defined as the glitch impulse transferred to the output of one converter due to a change in the DAC register code of another converter. It is specified in nV-s.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the digital inputs of the device can be capacitively coupled both across and through the device to appear as noise on the VOUT pins. It can also be coupled along the supply and ground lines. This noise is digital feedthrough.

Output Noise Spectral Density
Output noise spectral density is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per √Hz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in nV/√Hz.

THEORY OF OPERATION

DAC ARCHITECTURE

The AD5372/AD5373 contain 32 DAC channels and 32 output amplifiers in a single package. The architecture of a single DAC channel consists of a 16-bit (AD5372) or 14-bit (AD5373) resistor-string DAC followed by an output buffer amplifier. The resistor-string section is simply a string of resistors (of equal value) from VREF0 or VREF1 to AGND. This type of architecture guarantees DAC monotonicity. The 16-bit (AD5372) or 14-bit (AD5373) binary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before being fed into the output amplifier. The output amplifier multiplies the DAC output voltage by 4. The nominal output span is 12 V with a 3 V reference and 20 V with a 5 V reference.

CHANNEL GROUPS

The 32 DAC channels of the AD5372/AD5373 are arranged into four groups of eight channels. The eight DACs of Group 0 derive their reference voltage from VREF0. Group 1 to Group 3 derive their reference voltage from VREF1. Each group has its own signal ground pin.

Table 7. AD5372/AD5373 Registers

Register Name	Word Length in Bits	Description
X1A (Group) (Channel)	16 (14)	Input Data Register A, one for each DAC channel.
X1B (Group) (Channel)	16 (14)	Input Data Register B, one for each DAC channel.
M (Group) (Channel)	16 (14)	Gain trim registers, one for each DAC channel.
C (Group) (Channel)	16 (14)	Offset trim registers, one for each DAC channel.
X2A (Group) (Channel)	16 (14)	Output Data Register A, one for each DAC channel. These registers store the final, calibrated DAC data after gain and offset trimming. They are not readable or directly writable.
X2B (Group) (Channel)	16 (14)	Output Data Register B, one for each DAC channel. These registers store the final, calibrated DAC data after gain and offset trimming. They are not readable or directly writable.
DAC (Group) (Channel)		Data registers from which the DACs take their final input data. The DAC registers are updated from the X2A or X2B registers. They are not readable or directly writable.
OFS0	14	Offset DAC 0 data register: sets offset for Group 0.
OFS1	14	Offset DAC 1 data register: sets offset for Group 1 to Group 3.
Control	3	Bit 2 = $\overline{A}$/B. 0 = global selection of X1A input data registers. 1 = global selection of X1B input data registers. Bit 1 = enable thermal shutdown. 0 = disable thermal shutdown. 1 = enable thermal shutdown. Bit 0 = software power-down. 0 = software power-up. 1 = software power-down.
A/B Select 0	8	Each bit in this register determines whether a DAC in Group 0 takes its data from Register X2A or Register X2B (0 = X2A, 1 = X2B).
A/B Select 1	8	Each bit in this register determines whether a DAC in Group 1 takes its data from Register X2A or Register X2B (0 = X2A, 1 = X2B).
A/B Select 2	8	Each bit in this register determines whether a DAC in Group 2 takes its data from Register X2A or Register X2B (0 = X2A, 1 = X2B).
A/B Select 3	8	Each bit in this register determines whether a DAC in Group 3 takes its data from Register X2A or Register X2B (0 = X2A, 1 = X2B).

Table 8. AD5372/AD5373 Input Register Default Values

Register Name	AD5372 Default Value	AD5373 Default Value
X1A, X1B	0x5554	0x1555
M	0xFFFF	0x3FFF
C	0x8000	0x2000
OFS0, OFS1	0x1555	0x1555
Control	0x00	0x00
A/B Select 0 to A/B Select 3	0x00	0x00

A/B REGISTERS AND GAIN/OFFSET ADJUSTMENT

Each DAC channel has seven data registers. The actual DAC data-word can be written to either the X1A or the X1B input register, depending on the setting of the $\overline{A}$/B bit in the control register. If the $\overline{A}$/B bit is 0, data is written to the X1A register. If the $\overline{A}$/B bit is 1, data is written to the X1B register. Note that this single bit is a global control and affects every DAC channel in the device. It is not possible to set up the device on a per-channel basis so that some writes are to X1A registers and some writes are to X1B registers.

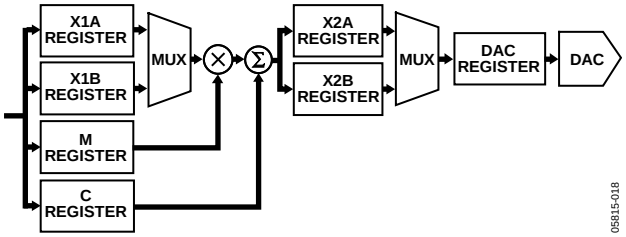


Figure 19. Data Registers Associated with Each DAC Channel

Each DAC channel also has a gain (M) register and an offset (C) register, which allow trimming out of the gain and offset errors of the entire signal chain. Data from the X1A register is operated on by a digital multiplier and adder controlled by the contents of the M and C registers. The calibrated DAC data is then stored in the X2A register. Similarly, data from the X1B register is operated on by the multiplier and adder and stored in the X2B register.

Although a multiplier and adder symbol are shown in Figure 19 for each channel, there is only one multiplier and one adder in the device, which are shared among all channels. This has implications for the update speed when several channels are updated at once, as described in the Register Update Rates section.

Each time data is written to the X1A register, or to the M or C register with the $\overline{A}$/B control bit set to 0, the X2A data is recalculated and the X2A register is automatically updated. Similarly, X2B is updated each time data is written to X1B, or to M or C with $\overline{A}$/B set to 1. The X2A and X2B registers are not readable or directly writable by the user.

Data output from the X2A and X2B registers is routed to the final DAC register by a multiplexer. Whether each individual DAC takes its data from the X2A or from the X2B register is controlled by an 8-bit A/B select register associated with each group of eight DACs. If a bit in this register is 0, the DAC takes its data from the X2A register; if 1, the DAC takes its data from the X2B register (Bit 0 through Bit 7 control DAC 0 to DAC 7).

Note that because there are 32 bits in four registers, it is possible to set up, on a per-channel basis, whether each DAC takes its data from the X2A or X2B register. A global command is also provided that sets all bits in the A/B select registers to 0 or to 1.

LOAD DAC

All DACs in the AD5372/AD5373 can be updated simultaneously by taking $\overline{LDAC}$ low when each DAC register is updated from either its X2A or X2B register, depending on the setting of the A/B select registers. The DAC register is not readable or directly writable by the user. $\overline{LDAC}$ can be permanently tied low, and the DAC output is updated whenever new data appears in the appropriate DAC register.

OFFSET DACs

In addition to the gain and offset trim for each DAC, there are two 14-bit offset DACs, one for Group 0 and one for Group 1 to Group 3. These allow the output range of all DACs connected to them to be offset within a defined range. Thus, subject to the limitations of headroom, it is possible to set the output range of Group 0 or Group 1 to Group 3 to be unipolar positive, unipolar negative, or bipolar, either symmetrical or asymmetrical about 0 V. The DACs in the AD5372/AD5373 are factory trimmed with the offset DACs set at their default values. This gives the best offset and gain performance for the default output range and span.

When the output range is adjusted by changing the value of the offset DAC, an extra offset is introduced due to the gain error of the offset DAC. The amount of offset is dependent on the magnitude of the reference and how much the offset DAC moves from its default value. See the Specifications section for this offset. The worst-case offset occurs when the offset DAC is at positive or negative full scale. This value can be added to the offset present in the main DAC channel to give an indication of the overall offset for that channel. In most cases, the offset can be removed by programming the C register of the channel with an appropriate value. The extra offset caused by the offset DAC needs to be taken into account only when the offset DAC is changed from its default value. Figure 20 shows the allowable code range that can be loaded to the offset DAC, depending on the reference value used. Thus, for a 5 V reference, the offset DAC should not be programmed with a value greater than 8192 (0x2000).

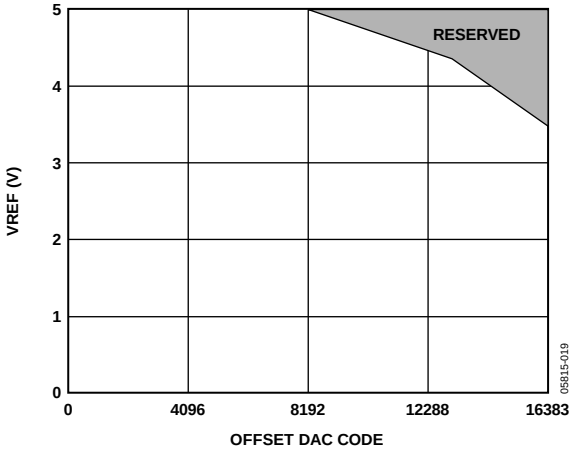


Figure 20. Offset DAC Code Range

OUTPUT AMPLIFIER

Because the output amplifiers can swing to 1.4 V below the positive supply and 1.4 V above the negative supply, this limits how much the output can be offset for a given reference voltage. For example, it is not possible to have a unipolar output range of 20 V, because the maximum supply voltage is ±16.5 V.

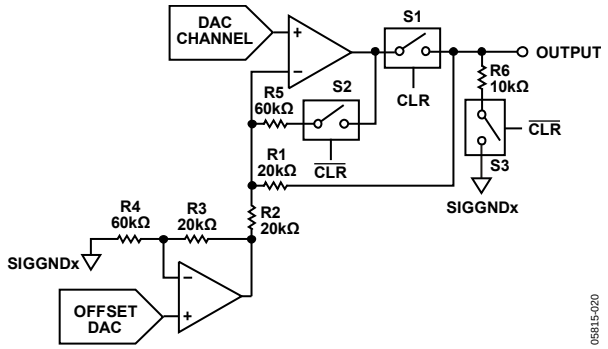


Figure 21. Output Amplifier and Offset DAC

Figure 21 shows details of a DAC output amplifier and its connections to the offset DAC. On power-up, S1 is open, disconnecting the amplifier from the output. S3 is closed, so the output is pulled to SIGGNDx (R1 and R2 are greater than R6). S2 is also closed to prevent the output amplifier from being open-loop. If $\overline{\text{CLR}}$ is low at power-up, the output remains in this condition until $\overline{\text{CLR}}$ is taken high. The DAC registers can be programmed, and the outputs assume the programmed values when $\overline{\text{CLR}}$ is taken high. Even if $\overline{\text{CLR}}$ is high at power-up, the output remains in the previous condition until V_{DD} > 6 V and V_{SS} < −4 V and the initialization sequence has finished. The outputs then go to their power-on default value.

TRANSFER FUNCTION

The output voltage of a DAC in the AD5372/AD5373 is dependent on the value in the input register, the value of the M and C registers, and the value in the offset DAC.

AD5372 Transfer Function

The input code is the value in the X1A or X1B register that is applied to the DAC (X1A, X1B default code = 21,844).

$$DAC_CODE = INPUT_CODE \times (M + 1)/2^{16} + C - 2^{15}$$

where:
M = code in gain register − default code = $2^{16} - 1$.
C = code in offset register − default code = 2^{15}.

The DAC output voltage is calculated as follows:

$$VOUT = 4 \times VREFx \times (DAC_CODE - (OFFSET_CODE \times 4))/2^{16} + V_{SIGGND}$$

where:
DAC_CODE should be within the range of 0 to 65,535.
For 12 V span, *VREFx* = 3.0 V.
For 20 V span, *VREFx* = 5.0 V.
OFFSET_CODE is the code loaded to the offset DAC. It is multiplied by 4 in the transfer function because this DAC is a 14-bit device. On power-up, the default code loaded to the offset DAC is 5461 (0x1555). With a 3 V reference, this gives a span of −4 V to +8 V.

AD5373 Transfer Function

The input code is the value in the X1A or X1B register that is applied to the DAC (X1A, X1B default code = 5461).

$$DAC_CODE = INPUT_CODE \times (M + 1)/2^{14} + C - 2^{13}$$

where:
M = code in gain register − default code = $2^{14} - 1$.
C = code in offset register − default code = 2^{13}.

The DAC output voltage is calculated as follows:

$$VOUT = 4 \times VREFx \times (DAC_CODE - OFFSET_CODE)/2^{14} + V_{SIGGND}$$

where:
DAC_CODE should be within the range of 0 to 16,383.
For 12 V span, *VREFx* = 3.0 V.
For 20 V span, *VREFx* = 5.0 V.
OFFSET_CODE is the code loaded to the offset DAC.
On power-up, the default code loaded to the offset DAC is 5461 (0x1555). With a 3 V reference, this gives a span of −4 V to +8 V.

REFERENCE SELECTION

The AD5372/AD5373 have two reference input pins. The voltage applied to the reference pins determines the output voltage span on VOUT0 to VOUT31. VREF0 determines the voltage span for VOUT0 to VOUT7 (Group 0), and VREF1 determines the voltage span for VOUT8 to VOUT31 (Group 1 to Group 3). The reference voltage applied to each VREF pin can be different, if required, allowing the groups to have different voltage spans. The output voltage range and span can be adjusted further by programming the offset and gain registers for each channel as well as programming the offset DACs. If the offset and gain features are not used (that is, the M and C registers are left at their default values), the required reference levels can be calculated as follows:

$$VREF = (VOUT_{MAX} - VOUT_{MIN})/4$$

If the offset and gain features of the AD5372/AD5373 are used, the required output range is slightly different. The selected output range should take into account the system offset and gain errors that need to be trimmed out. Therefore, the selected output range should be larger than the actual required range.

The required reference levels can be calculated as follows:

1. Identify the nominal output range on VOUT.
2. Identify the maximum offset span and the maximum gain required on the full output signal range.
3. Calculate the new maximum output range on VOUT, including the expected maximum offset and gain errors.
4. Choose the new required $VOUT_{MAX}$ and $VOUT_{MIN}$, keeping the VOUT limits centered on the nominal values. Note that V_{DD} and V_{SS} must provide sufficient headroom.
5. Calculate the value of VREF as follows:

$$VREF = (VOUT_{MAX} - VOUT_{MIN})/4$$

Reference Selection Example

If

Nominal output range = 12 V (−4 V to +8 V)

Zero-scale error = ±70 mV

Gain error = ±3%, and

SIGGNDx = AGND = 0 V

Then

Gain error = ±3%
=> Maximum positive gain error = 3%
=> Output range including gain error = 12 + 0.03(12) = 12.36 V

Zero-scale error = ±70 mV
=> Maximum offset error span = 2(70 mV) = 0.14 V
=> Output range including gain error and zero-scale error = 12.36 V + 0.14 V = 12.5 V

VREF calculation
Actual output range = 12.5 V, that is, −4.25 V to +8.25 V;
VREF = (8.25 V + 4.25 V)/4 = 3.125 V

If the solution yields an inconvenient reference level, the user can adopt one of the following approaches:

- Use a resistor divider to divide down a convenient, higher reference level to the required level.
- Select a convenient reference level above VREF and modify the gain and offset registers to digitally downsize the reference. In this way, the user can use almost any convenient reference level but can reduce the performance by overcompaction of the transfer function.
- Use a combination of these two approaches.

CALIBRATION

The user can perform a system calibration on the AD5372/AD5373 to reduce gain and offset errors to below 1 LSB. This reduction is achieved by calculating new values for the M and C registers and reprogramming them.

The M and C registers should not be programmed until both the zero-scale and full-scale errors are calculated.

Reducing Zero-Scale Error

Zero-scale error can be reduced as follows:

1. Set the output to the lowest possible value.
2. Measure the actual output voltage and compare it to the required value. This gives the zero-scale error.
3. Calculate the number of LSBs equivalent to the error and add this number to the default value of the C register. Note that only negative zero-scale error can be reduced.

Reducing Full-Scale Error

Full-scale error can be reduced as follows:

1. Measure the zero-scale error.
2. Set the output to the highest possible value.
3. Measure the actual output voltage and compare it to the required value. Add this error to the zero-scale error. This is the span error, which includes the full-scale error.
4. Calculate the number of LSBs equivalent to the span error and subtract this number from the default value of the M register. Note that only positive full-scale error can be reduced.

AD5372 Calibration Example

This example assumes that a −4 V to +8 V output is required. The DAC output is set to −4 V but is measured at −4.03 V. This gives a zero-scale error of −30 mV.

1 LSB = 12 V/65,536 = 183.105 µV

30 mV = 164 LSBs

The full-scale error can now be calculated. The output is set to 8 V and a value of 8.02 V is measured. This gives a full-scale error of +20 mV and a span error of +20 mV − (−30 mV) = +50 mV.

50 mV = 273 LSBs

The errors can now be removed as follows:

1. Add 164 LSBs to the default C register value: (32,768 + 164) = 32,932
2. Subtract 273 LSBs from the default M register value: (65,535 − 273) = 65,262
3. Program the M register to 65,262; program the C register to 32,932.

ADDITIONAL CALIBRATION

The techniques described in the previous section are usually enough to reduce the zero-scale and full-scale errors in most applications. However, there are limitations whereby the errors may not be sufficiently reduced. For example, the offset (C) register can only be used to reduce the offset caused by the negative zero-scale error. A positive offset cannot be reduced. Likewise, if the maximum voltage is below the ideal value, that is, a negative full-scale error, the gain (M) register cannot be used to increase the gain to compensate for the error.

These limitations can be overcome by increasing the reference value. With a 3 V reference, a 12 V span is achieved. The ideal voltage range, for the AD5372 or the AD5373, is −4 V to +8 V. Using a +3.1 V reference increases the range to −4.133 V to +8.2667 V. Clearly, in this case, the offset and gain errors are insignificant, and the M and C registers can be used to raise the negative voltage to −4 V and then reduce the maximum voltage to +8 V to give the most accurate values possible.

RESET FUNCTION

The reset function is initiated by the $\overline{\text{RESET}}$ pin. On the rising edge of $\overline{\text{RESET}}$, the AD5372/AD5373 state machine initiates a reset sequence to reset the X, M, and C registers to their default values. This sequence typically takes 300 µs, and the user should not write to the part during this time. On power-up, it is recommended that the user bring $\overline{\text{RESET}}$ high as soon as possible to properly initialize the registers.

When the reset sequence is complete (and provided that $\overline{\text{CLR}}$ is high), the DAC output is at a potential specified by the default register settings, which is equivalent to SIGGNDx. The DAC outputs remain at SIGGNDx until the X, M, or C register is updated and $\overline{\text{LDAC}}$ is taken low. The AD5372/AD5373 can be returned to the default state by pulsing $\overline{\text{RESET}}$ low for at least 30 ns. Note that, because the reset function is triggered by the rising edge, bringing $\overline{\text{RESET}}$ low has no effect on the operation of the AD5372/AD5373.

CLEAR FUNCTION

$\overline{\text{CLR}}$ is an active low input that should be high for normal operation. The $\overline{\text{CLR}}$ pin has an internal 500 kΩ pull-down resistor. When $\overline{\text{CLR}}$ is low, the input to each of the DAC output buffer stages (VOUT0 to VOUT31) is switched to the externally set potential on the relevant SIGGNDx pin. While $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is taken high again, the DAC outputs return to their previous values. The contents of the input registers and DAC Register 0 to DAC Register 31 are not affected by taking $\overline{\text{CLR}}$ low. To prevent glitches from appearing on the outputs, $\overline{\text{CLR}}$ should be brought low whenever the output span is adjusted by writing to the offset DAC.

$\overline{\text{BUSY}}$ AND $\overline{\text{LDAC}}$ FUNCTIONS

The value of an X2 (A or B) register is calculated each time the user writes new data to the corresponding X1, C, or M register. During the calculation of X2, the $\overline{\text{BUSY}}$ output goes low. While $\overline{\text{BUSY}}$ is low, the user can continue writing new data to the X1, M, or C register (see the Register Update Rates section for more details), but no DAC output updates can take place.

The $\overline{\text{BUSY}}$ pin is bidirectional and has a 50 kΩ internal pull-up resistor. When multiple AD5372 or AD5373 devices are used in one system, the $\overline{\text{BUSY}}$ pins can be tied together. This is useful when it is required that no DAC in any device be updated until all other DACs are ready. When each device has finished updating the X2 (A or B) registers, it releases the $\overline{\text{BUSY}}$ pin. If another device has not finished updating its X2 registers, it holds $\overline{\text{BUSY}}$ low, thus delaying the effect of $\overline{\text{LDAC}}$ going low.

The DAC outputs are updated by taking the $\overline{\text{LDAC}}$ input low. If $\overline{\text{LDAC}}$ goes low while $\overline{\text{BUSY}}$ is active, the $\overline{\text{LDAC}}$ event is stored and the DAC outputs are updated immediately after $\overline{\text{BUSY}}$ goes high. A user can also hold the $\overline{\text{LDAC}}$ input permanently low. In this case, the DAC outputs are updated immediately after $\overline{\text{BUSY}}$ goes high. Whenever the A/B select registers are written to, $\overline{\text{BUSY}}$ also goes low, for approximately 500 ns.

The AD5372/AD5373 have flexible addressing that allows writing of data to a single channel, all channels in a group, the same channel in Group 0 to Group 3, the same channel in Group 1 to Group 3, or all channels in the device. This means that 1, 4, 8, or 32 DAC register values may need to be calculated and updated. Because there is only one multiplier shared among 32 channels, this task must be done sequentially so that the length of the $\overline{\text{BUSY}}$ pulse varies according to the number of channels being updated.

Table 9. $\overline{\text{BUSY}}$ Pulse Widths

Action	$\overline{\text{BUSY}}$ Pulse Width[1]
Loading input, C, or M to 1 channel[2]	1.5 µs maximum
Loading input, C, or M to 4 channels	3.3 µs maximum
Loading input, C, or M to 8 channels	5.7 µs maximum
Loading input, C, or M to 32 channels	20.1 µs maximum

[1] $\overline{\text{BUSY}}$ pulse width = ((number of channels + 1) × 600 ns) + 300 ns.
[2] A single channel update is typically 1 µs.

The AD5372/AD5373 contain an extra feature whereby a DAC register is not updated unless its X2A or X2B register has been written to since the last time $\overline{\text{LDAC}}$ was brought low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers are filled with the contents of the X2A or X2B register, depending on the setting of the A/B select registers. However, the AD5372/AD5373 update the DAC register only if the X2A or X2B data has changed, thereby removing unnecessary digital crosstalk.

POWER-DOWN MODE

The AD5372/AD5373 can be powered down by setting Bit 0 in the control register to 1. This turns off the DACs, thus reducing the current consumption. The DAC outputs are connected to their respective SIGGNDx potentials. The power-down mode does not change the contents of the registers, and the DACs return to their previous voltage when the power-down bit is cleared to 0.

THERMAL SHUTDOWN FUNCTION

The AD5372/AD5373 can be programmed to shut down the DACs if the temperature on the die exceeds 130°C. Setting Bit 1 in the control register to 1 enables this function (see Table 16). If the die temperature exceeds 130°C, the AD5372/AD5373 enter a thermal shutdown mode, which is equivalent to setting the power-down bit in the control register to 1. To indicate that the AD5372/AD5373 have entered thermal shutdown mode, Bit 4 of the control register is set to 1. The AD5372/AD5373 remain in thermal shutdown mode, even if the die temperature falls, until Bit 1 in the control register is cleared to 0.

TOGGLE MODE

The AD5372/AD5373 have two X2 registers per channel, X2A and X2B, which can be used to switch the DAC output between two levels with ease. This approach greatly reduces the overhead required by a microprocessor, which would otherwise need to write to each channel individually. When the user writes to the X1A, X1B, M, or C register, the calculation engine takes a certain amount of time to calculate the appropriate X2A or X2B value. If an application, such as a data generator, requires that the DAC output switch between two levels only, any method that reduces the amount of calculation time necessary is advantageous. For the data generator example, the user needs only to set the high and low levels for each channel once by writing to the X1A and X1B registers. The values of X2A and X2B are calculated and stored in their respective registers. The calculation delay, therefore, happens only during the setup phase, that is, when programming the initial values. To toggle a DAC output between the two levels, it is only required to write to the relevant A/B select register to set the MUX2 register bit. Furthermore, because there are eight MUX2 control bits per register, it is possible to update eight channels with a single write. Table 10 shows the bits that correspond to each DAC output.

Table 10. DACs Selected by A/B Select Registers

A/B Select Register	Bits[1]							
	F7	F6	F5	F4	F3	F2	F1	F0
0	VOUT7	VOUT6	VOUT5	VOUT4	VOUT3	VOUT2	VOUT1	VOUT0
1	VOUT15	VOUT14	VOUT13	VOUT12	VOUT11	VOUT10	VOUT9	VOUT8
2	VOUT23	VOUT22	VOUT21	VOUT20	VOUT19	VOUT18	VOUT17	VOUT16
3	VOUT31	VOUT30	VOUT29	VOUT28	VOUT27	VOUT26	VOUT25	VOUT24

[1] If the bit is set to 0, Register X2A is selected. If the bit is set to 1, Register X2B is selected.

SERIAL INTERFACE

The AD5372/AD5373 contain a high speed SPI operating at clock frequencies up to 50 MHz (20 MHz for read operations). To minimize both the power consumption of the device and on-chip digital noise, the interface powers up fully only when the device is being written to, that is, on the falling edge of $\overline{SYNC}$. The serial interface is 2.5 V LVTTL-compatible when operating from a 2.5 V to 3.6 V DV_{CC} supply. It is controlled by four pins: $\overline{SYNC}$ (frame synchronization input), SDI (serial data input pin), SCLK (clocks data in and out of the device), and SDO (serial data output pin for data readback).

SPI WRITE MODE

The AD5372/AD5373 allow writing of data via the serial interface to every register directly accessible to the serial interface, that is, all registers except the X2A, X2B, and DAC registers. The X2A and X2B registers are updated when writing to the X1A, X1B, M, and C registers, and the DAC data registers are updated by $\overline{LDAC}$. The serial word (see Table 11 or Table 12) is 24 bits long: 16 (AD5372) or 14 (AD5373) of these bits are data bits; six bits are address bits; and two bits are mode bits that determine what is done with the data. Two bits are reserved on the AD5373.

The serial interface works with both a continuous and a burst (gated) serial clock. Serial data applied to SDI is clocked into the AD5372/AD5373 by clock pulses applied to SCLK. The first falling edge of $\overline{SYNC}$ starts the write cycle. At least 24 falling clock edges must be applied to SCLK to clock in 24 bits of data before $\overline{SYNC}$ is taken high again. If $\overline{SYNC}$ is taken high before the 24th falling clock edge, the write operation is aborted.

If a continuous clock is used, $\overline{SYNC}$ must be taken high before the 25th falling clock edge. This inhibits the clock within the AD5372/AD5373. If more than 24 falling clock edges are applied before $\overline{SYNC}$ is taken high again, the input data becomes corrupted. If an externally gated clock of exactly 24 pulses is used, $\overline{SYNC}$ can be taken high any time after the 24th falling clock edge.

The input register addressed is updated on the rising edge of $\overline{SYNC}$. For another serial transfer to take place, $\overline{SYNC}$ must be taken low again.

SPI READBACK MODE

The AD5372/AD5373 allow data readback via the serial interface from every register directly accessible to the serial interface, that is, all registers except the X2A, X2B, and DAC data registers. To read back a register, it is first necessary to tell the AD5372/AD5373 which register is to be read. This is achieved by writing a word whose first two bits are the Special Function Code 00 to the device. The remaining bits then determine which register is to be read back.

If a readback command is written to a special function register, data from the selected register is clocked out of the SDO pin during the next SPI operation. The SDO pin is normally three-stated but becomes driven as soon as a read command is issued. The pin remains driven until the register data is clocked out. See Figure 5 for the read timing diagram. Note that due to the timing requirements of t_{22} (25 ns), the maximum speed of the SPI interface during a read operation should not exceed 20 MHz.

REGISTER UPDATE RATES

The value of the X2A register or the X2B register is calculated each time the user writes new data to the corresponding X1, C, or M register. The calculation is performed by a three-stage process. The first two stages take approximately 600 ns each, and the third stage takes approximately 300 ns. When the write to an X1, C, or M register is complete, the calculation process begins. If the write operation involves the update of a single DAC channel, the user is free to write to another register, provided that the write operation does not finish until the first-stage calculation is complete (that is, 600 ns after the completion of the first write operation). If a group of channels is being updated by a single write operation, the first-stage calculation is repeated for each channel, taking 600 ns per channel. In this case, the user should not complete the next write operation until this time has elapsed.

Table 11. AD5372 Serial Word Bit Assignment

I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
M1	M0	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 12. AD5373 Serial Word Bit Assignment

I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1[1]	I0[1]
M1	M0	A5	A4	A3	A2	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0

[1] Bit I1 and Bit I0 are reserved for future use and should be 0 when writing the serial word. These bits read back as 0.

CHANNEL ADDRESSING AND SPECIAL MODES

If the mode bits are not 00, the data-word D15 to D0 (AD5372) or D13 to D0 (AD5373) is written to the device. Address Bit A5 to Address Bit A0 determine which channels are written to, and the mode bits determine to which register (X1A, X1B, C, or M) the data is written, as shown in Table 13 and Table 14. Data is to be written to the X1A register when the $\overline{A}$/B bit in the control register is 0, or to the X1B register when the $\overline{A}$/B bit is 1.

The AD5372/AD5373 have very flexible addressing that allows the writing of data to a single channel, all channels in a group, the same channel in Group 0 to Group 3, the same channel in Group 1 to Group 3, or all channels in the device. Table 14 shows which groups and which channels are addressed for every combination of Address Bit A5 to Address Bit A0.

Table 13. Mode Bits

M1	M0	Action
1	1	Write to DAC data (X) register
1	0	Write to DAC offset (C) register
0	1	Write to DAC gain (M) register
0	0	Special function, used in combination with other bits of the data-word

Table 14. Group and Channel Addressing

Address Bit A2 to Address Bit A0	Address Bit A5 to Address Bit A3							
	000	001	010	011	100	101	110	111
000	All groups, all channels	Group 0, Channel 0	Group 1, Channel 0	Group 2, Channel 0	Group 3, Channel 0	Reserved	Group 0, Group 1, Group 2, Group 3; Channel 0	Group 1, Group 2, Group 3; Channel 0
001	Group 0, all channels	Group 0, Channel 1	Group 1, Channel 1	Group 2, Channel 1	Group 3, Channel 1	Reserved	Group 0, Group 1, Group 2, Group 3; Channel 1	Group 1, Group 2, Group 3; Channel 1
010	Group 1, all channels	Group 0, Channel 2	Group 1, Channel 2	Group 2, Channel 2	Group 3, Channel 2	Reserved	Group 0, Group 1, Group 2, Group 3; Channel 2	Group 1, Group 2, Group 3; Channel 2
011	Group 2, all channels	Group 0, Channel 3	Group 1, Channel 3	Group 2, Channel 3	Group 3, Channel 3	Reserved	Group 0, Group 1, Group 2, Group 3; Channel 3	Group 1, Group 2, Group 3; Channel 3
100	Group 3, all channels	Group 0, Channel 4	Group 1, Channel 4	Group 2, Channel 4	Group 3, Channel 4	Reserved	Group 0, Group 1, Group 2, Group 3; Channel 4	Group 1, Group 2, Group 3; Channel 4
101	Reserved	Group 0, Channel 5	Group 1, Channel 5	Group 2, Channel 5	Group 3, Channel 5	Reserved	Group 0, Group 1, Group 2, Group 3; Channel 5	Group 1, Group 2, Group 3; Channel 5
110	Reserved	Group 0, Channel 6	Group 1, Channel 6	Group 2, Channel 6	Group 3, Channel 6	Reserved	Group 0, Group 1, Group 2, Group 3; Channel 6	Group 1, Group 2, Group 3; Channel 6
111	Reserved	Group 0, Channel 7	Group 1, Channel 7	Group 2, Channel 7	Group 3, Channel 7	Reserved	Group 0, Group 1, Group 2, Group 3; Channel 7	Group 1, Group 2, Group 3; Channel 7

SPECIAL FUNCTION MODE

If the mode bits are 00, then the special function mode is selected, as shown in Table 15. Bit I21 to Bit I16 of the serial data-word select the special function, and the remaining bits are data required for execution of the special function, for example, the channel address for data readback. The codes for the special functions are shown in Table 16. Table 17 shows the addresses for data readback.

Table 15. Special Function Mode

I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
0	0	S5	S4	S3	S2	S1	S0	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

Table 16. Special Function Codes

Special Function Code							
S5	S4	S3	S2	S1	S0	Data (F15 to F0)	Action
0	0	0	0	0	0	0000 0000 0000 0000	NOP.
0	0	0	0	0	1	XXXX XXXX XXXX X[F2:F0]	Write control register. F4 = overtemperature indicator (read-only bit). This bit should be 0 when writing to the control register. F3 = reserved. This bit should be 0 when writing to the control register. F2 = 1: Select Register X1B for input. F2 = 0: Select Register X1A for input. F1 = 1: Enable thermal shutdown mode. F1 = 0: Disable thermal shutdown mode. F0 = 1: Software power-down. F0 = 0: Software power-up.
0	0	0	0	1	0	XX[F13:F0]	Write data in F13 to F0 to OFS0 register.
0	0	0	0	1	1	XX[F13:F0]	Write data in F13 to F0 to OFS1 register.
0	0	0	1	0	0	Reserved	
0	0	0	1	0	1	See Table 17	Select register for readback.
0	0	0	1	1	0	XXXX XXXX [F7:F0]	Write data in F7 to F0 to A/B Select Register 0.
0	0	0	1	1	1	XXXX XXXX [F7:F0]	Write data in F7 to F0 to A/B Select Register 1.
0	0	1	0	0	0	XXXX XXXX [F7:F0]	Write data in F7 to F0 to A/B Select Register 2.
0	0	1	0	0	1	XXXX XXXX [F7:F0]	Write data in F7 to F0 to A/B Select Register 3.
0	0	1	0	1	0	Reserved	
0	0	1	0	1	1	XXXX XXXX [F7:F0]	Block write to A/B select registers. F7 to F0 = 0: Write all 0s (all channels use the X2A register). F7 to F0 = 1: Write all 1s (all channels use the X2B register).

Table 17. Address Codes for Data Readback[1]

F15	F14	F13	F12	F11	F10	F9	F8	F7	Register Read
0	0	0	Bit F12 to Bit F7 select the channel to be read back, from Channel 0 = 001000 to Channel 31 = 100111						X1A register
0	0	1							X1B register
0	1	0							C register
0	1	1							M register
1	0	0	0	0	0	0	0	1	Control register
1	0	0	0	0	0	0	1	0	OFS0 data register
1	0	0	0	0	0	0	1	1	OFS1 data register
1	0	0	0	0	0	1	0	0	Reserved
1	0	0	0	0	0	1	1	0	A/B Select Register 0
1	0	0	0	0	0	1	1	1	A/B Select Register 1
1	0	0	0	0	1	0	0	0	A/B Select Register 2
1	0	0	0	0	1	0	0	1	A/B Select Register 3
1	0	0	0	0	1	0	1	0	Reserved

[1] Bit F6 to Bit F0 are don't cares for the data readback function.

APPLICATIONS INFORMATION

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit boards on which the AD5372/AD5373 are mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5372/AD5373 are in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. For supplies with multiple pins (V_{SS}, V_{DD}, DV_{CC}), it is recommended that these pins be tied together and that each supply be decoupled only once.

The AD5372/AD5373 should have ample supply decoupling of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI)—typical of the common ceramic types that provide a low impedance path to ground at high frequencies—to handle transient currents due to internal logic switching.

Digital lines running under the device should be avoided because they can couple noise onto the device. The analog ground plane should be allowed to run under the AD5372/AD5373 to avoid noise coupling. The power supply lines of the AD5372/AD5373 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching digital signals should be shielded with digital ground to avoid radiating noise to other parts of the board, and they should never be run near the reference inputs. It is essential to minimize noise on the VREF0 and VREF1 lines.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best approach, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, while signal traces are placed on the solder side.

As is the case for all thin packages, care must be taken to avoid flexing the package and to avoid a point load on the surface of this package during the assembly process.

POWER SUPPLY SEQUENCING

When the supplies are connected to the AD5372/AD5373, it is important that the AGND and DGND pins be connected to the relevant ground plane before the positive or negative supplies are applied. In most applications, this is not an issue because the ground pins for the power supplies are connected to the ground pins of the AD5372/AD5373 via ground planes. When the AD5372/AD5373 are to be used in a hot-swap card, care should be taken to ensure that the ground pins are connected to the supply grounds before the positive or negative supplies are connected. This is required to prevent currents from flowing in directions other than toward an analog or digital ground.

INTERFACING EXAMPLES

The SPI interface of the AD5372/AD5373 is designed to allow the parts to be easily connected to industry-standard DSPs and microcontrollers. Figure 22 shows how the AD5372/AD5373 connects to the Analog Devices, Inc., Blackfin® DSP. The Blackfin has an integrated SPI port that can be connected directly to the SPI pins of the AD5372/AD5373 and programmable I/O pins that can be used to set or read the state of the digital input or output pins associated with the interface.

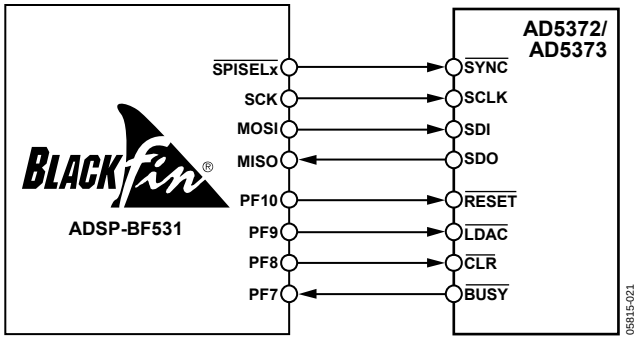


Figure 22. Interfacing to a Blackfin DSP

The Analog Devices ADSP-21065L is a floating-point DSP with two serial ports (SPORTs). Figure 23 shows how one SPORT can be used to control the AD5372/AD5373. In this example, the transmit frame synchronization (TFSx) pin is connected to the receive frame synchronization (RFSx) pin. Similarly, the transmit and receive clocks (TCLKx and RCLKx) are also connected. The user can write to the AD5372/AD5373 by writing to the transmit register of the ADSP-21065L. A read operation can be accomplished by first writing to the AD5372/AD5373 to tell the part that a read operation is required. A second write operation with an NOP instruction causes the data to be read from the AD5372/AD5373. The DSP receive interrupt can be used to indicate when the read operation is complete.

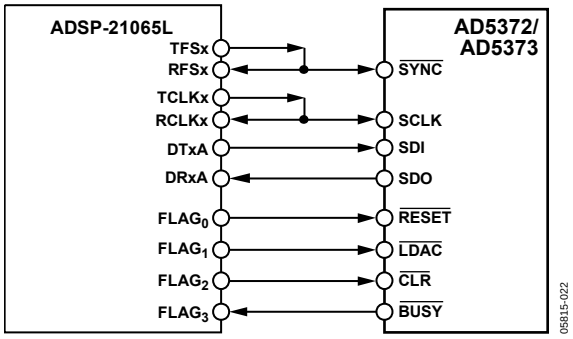
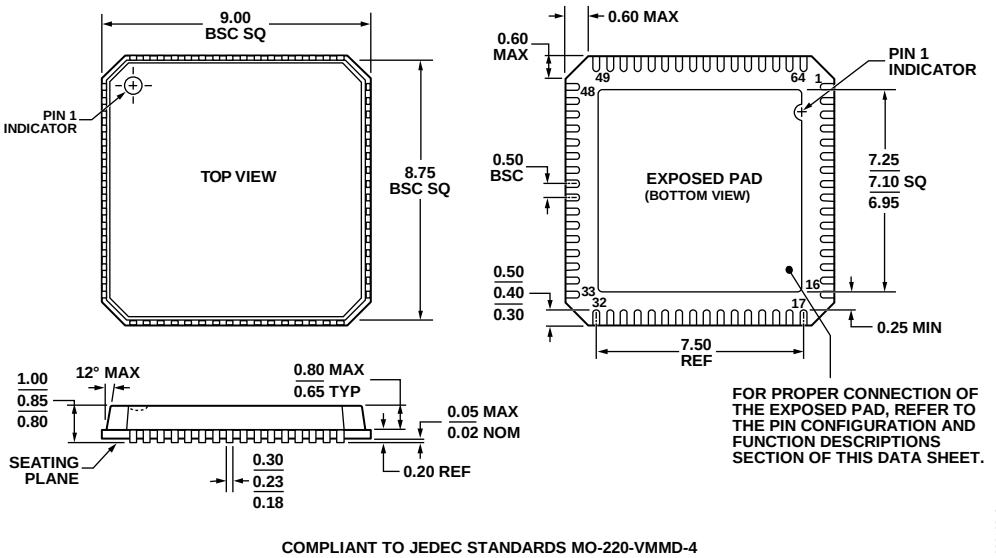


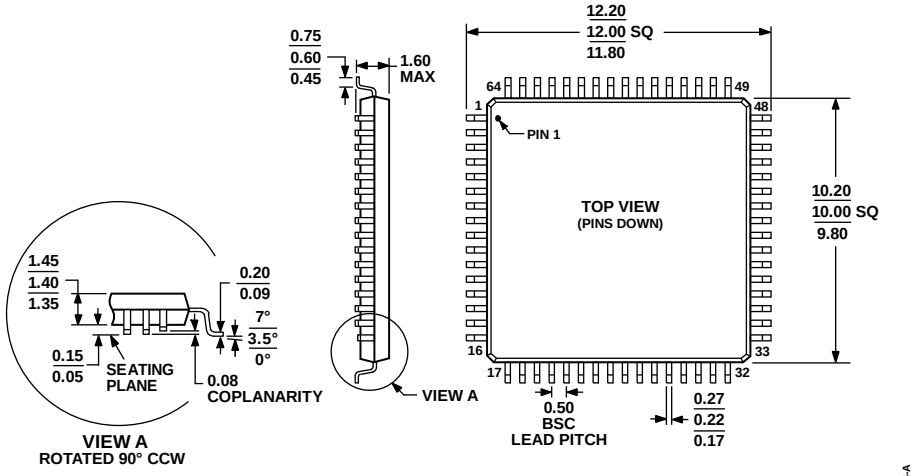
Figure 23. Interfacing to an ADSP-21065L DSP

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4

Figure 24. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-3)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-BCD

Figure 25. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD5372BSTZ	−40°C to +85°C	64-Lead Low Profile Quad Flat Package (LQFP)	ST-64-2
AD5372BSTZ-REEL	−40°C to +85°C	64-Lead Low Profile Quad Flat Package (LQFP)	ST-64-2
AD5372BCPZ	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-3
AD5372BCPZ-RL7	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-3
AD5373BSTZ	−40°C to +85°C	64-Lead Low Profile Quad Flat Package (LQFP)	ST-64-2
AD5373BSTZ-REEL	−40°C to +85°C	64-Lead Low Profile Quad Flat Package (LQFP)	ST-64-2
AD5373BCPZ	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-3
AD5373BCPZ-RL7	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-3
EVAL-AD5372EBZ		Evaluation Board	
EVAL-AD5373EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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